

What is claimed is:

1 1. A vision system, comprising:
2 a pixel array having an array of pixels, said array of
3 pixels configured to receive light signals from an image having
4 at least one tracking target;

5 at least one multi-resolution window operation circuit
6 configured to process said image, each of said at least one
7 multi-resolution window operation circuit operating to process
8 each of said at least one tracking target within a particular
9 multi-resolution window; and

10 a pixel averaging circuit configured to sample and average
11 pixels within said particular multi-resolution window.

1 2. The system of claim 1, further comprising:
2 a target detection circuit configured to receive and process
3 said image such that said each of said at least one tracking
4 target is assigned to said particular multi-resolution window.

1 3. The system of claim 1, wherein said multi-resolution
2 window has a size between 1x1 and 32x32 pixels.

1 4. The system of claim 1, wherein said pixel averaging
2 circuit includes a plurality of column-parallel capacitors.

1 5. The system of claim 1, further comprising:
2 at least one output analog signal chain, each of said at
3 least one output analog signal chain configured to output signal
4 from said particular multi-resolution window.

1 6. The system of claim 5, further comprising:
2 a plurality of latches, each latch configured to hold
3 definition values of said particular multi-resolution window.

1 7. The system of claim 1, wherein each of said array
2 pixels includes a poly-silicon gate biased in deep-depletion.

1 8. The system of claim 1, wherein said pixel averaging
2 circuit includes a super-pixel configuration element that
3 operates to sequentially average the pixels within a super-pixel,
4 where said super-pixel is a group of pixels that is at least 2x2
5 pixels in size.

1 9. The system of claim 8, wherein each of said at least
2 one multi-resolution window operation circuit includes:

3 a super-pixel average address generation circuit configured
4 to generate addresses of pixels within said super-pixel;

5 a mask generation circuit operating to provide a mask
6 pattern for averaging pixels;

7 a switch network configured to input super-pixel averaging
8 address;

9 a super-pixel average address and row dump address
10 generation block operating provide average address and row dump
11 address to said pixel averaging circuit; and

12 a capacitor bank control signal generation block configured
13 to generate control signal for said pixel averaging circuit

1 10. The system of claim 9, wherein said switch network
2 includes $32 \times n$ switches, where n is a total number of columns.

1 11. The system of claim 10, wherein said switch network
2 includes a diagonal control connection to ensure that averaging
3 bit pattern is applied column-wise.

1 12. The system of claim 1, further comprising:
2 row and column control circuits operating to appropriately
3 arrange said light signal received by said pixel array.

1 13. The system of claim 10, wherein said column control
2 circuit further includes shift registers to shift and align each
3 column of said pixel array to an actual starting address within
4 said particular multi-resolution window.

1 14. A method for searching and tracking targets,
2 comprising:

3 receiving light signals from an image having at least one
4 tracking target;

5 detecting and separating said at least one tracking target
6 into at least one region of interest;

7 grouping each of said at least one region of interest into a
8 plurality of blocks; and

9 first averaging pixels within each of said plurality of
10 blocks.

1 15. The method of claim 14, where said first averaging
2 includes sequentially averaging the pixels within a super-pixel,
3 where said super-pixel is a group of pixels that is at least 2x2
4 pixels in size.

1 16. The method of claim 14, wherein said first averaging is
2 carried out in a passive capacitor array organized in column-
3 parallel fashion.

1 17. The method of claim 14, wherein said first averaging
2 includes block-averaging, said block-averaging including:
3 second averaging of a given row of pixel values;
4 storing an averaged value;
5 repeating said second averaging and storing for all rows,
6 said repeating generating a plurality of row averages; and
7 computing an average of said plurality of row averages.

1 18. The method of claim 17, wherein said computing includes
2 switching sample and hold capacitor in each column.

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